Kadi Sarva Vishwavidyalaya

Faculty of Engineering & Technology

Second Year Bachelor of Engineering (CE/IT) – Semester IV

(With effect from: Academic Year 2018-19)

Subject Code: CT403-N	**Subject Title:** Computer Organization & Architecture
Pre-requisite	

Teaching Scheme (Credits and Hours)

Teaching Scheme				Total Credit	Evaluation Scheme					
L	T	P	Total		Theory		Mid Sem Exam	CIA	Practical	Total
Hours	Hours	Hours	Hours		Hours	Marks	Marks	Marks	Marks	Marks
04	00	02	06	05	03	70	30	20	30	150

Learning Objectives:

- To understand the basic organization of modern computer systems and how computer programs are organized, stored, and executed at the machine level.
- To analyze an instruction-set architecture and propose a data path and control unit implementation.
- To understand how instruction pipelining enhances processor performance.
- To understand the basic organization of the memory hierarchy.
- To understand the input/output mechanisms used to connect computers to their external environment.
- To understand size of instructions and memory word for computer architectures.

Outline of the Course:

Sr. No	Title of the Unit	Minimum Hours
1	Overview of Register Transfer And Micro-operations	07
2	Basic Computer Organization And Design	13
3	Programming the Basic Computer	11
4	Central Processing Unit	11
5	Pipeline Processing	11
6	Memory Organization	11
	Total	**64**

Total hours (Theory): 64
Total hours (Lab): 32
Total hours: 96

Detailed Syllabus:

Sr. No	Topic	Lecture Hours	Weightage (%)
1	**Overview of Register Transfer And Micro operations** Register Transfer Language, Register transfer. Bus and Memory transfer**,** Arithmetic Micro-operations. Logic Micro-operations**,** Shift Micro-operations, Arithmetic Logic Shift Unit	07	12
2	**Basic Computer Organization And Design:** Instruction codes, Computer registers, Computer instructions, Timing and Control, Instruction cycle, Memory-Reference Instructions, Input-output and interrupt, Design of Basic computer, Design of Accumulator Unit.	13	20
3	**Programming the Basic Computer:** Introduction, Machine Language, Assembly Language and Assembler, Program loops, Programming Arithmetic and logic operations, Subroutines, I-O Programming.	11	17
4	**Central Processing Unit:** Introduction, General Register Organization, Stack Organization, Instruction format, Addressing Modes Data transfer and manipulation, Program Control, Reduced Instruction Set Computer (RISC).	11	17
5	**Pipeline Processing:** Parallel Processing ,Pipelining, Arithmetic Pipeline Instruction Pipeline, RISC Pipeline	11	17
6	**Memory Organization:** Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory	11	17
	Total	64	100

Instructional Method and Pedagogy:

- At the start of course, the course delivery pattern, prerequisite of the subject will be discussed.
- Lectures will be conducted with the aid of multi-media projector, black board, OHP etc.
- Attendance is compulsory in lecture and laboratory which carries 10 marks in overall evaluation.
- One internal exam will be conducted as a part of internal theory evaluation.
- Assignments based on the course content will be given to the students for each unit and will be evaluated at regular interval evaluation.
- Surprise tests/Quizzes/Seminar/tutorial will be conducted having a share of five marks in the overall internal evaluation.
- The course includes a laboratory, where students have an opportunity to build an appreciation for the concepts being taught in lectures.
- Experiments shall be performed in the laboratory related to course contents.

Learning Outcome:

On successful completion of this course, the student will:

- Be able to understand and design the basic computer architecture.
- Become familiar with micro-operations, instruction writing and role of micro instructions.
- Be able to understand the role of memory and its hierarchy.
- Be able to understand the principle of pipelining and the interdependencies between pipelining and instruction set design.
- Be able to understand the size of memory word and instruction length for different computer architectures.

E-Resources:

- http://nptel.ac.in/courses/106103068/
- https://users.ece.cmu.edu/~omutlu/lecture-videos.html
- http://nptel.ac.in/courses/106103068/pdf/coa.pdf

Reference Books:

1. Computer System Architecture: By M. Morris Mano.
2. Computer Organization by Hamacher et al. McGraw Hill Education.
3. Structured Computer Organization: By Tanenbaum.
4. Computer Organization: By Stallings.
5. Computer Architecture and Organization: By Hayes
6. Microprocessor Architecture, Programming, and Applications with the 8085 - Ramesh S. Gaonkar Pub: Penram International.

List of experiments:

Sr. No.	Name of Experiment
1	Study of Different Simulators
2	Design of Ripple Carry Adders
3	Design of Carry Lookahead Adders
4	Design of Registers and Counters
5	Design of Wallace Tree Adders
6	Design of Combinational Multiplier
7	Study and design of Booth's Multiplier
8	Design of ALU
9	Design of Memory
10	Design of Associative Cache
11	Design of Direct Mapped Cache
12	Study of CPU Design
	As part of experimentation, a small project / model / seminar / poster / other should be prepared / presented by student(s) based on the practical knowledge gained by this course at the end of the curriculum. The concerned laboratory faculty (in consultation with course coordinator) is empowered to design/decide the type/execution of this experiment. The student(s) are expected to present the same before their batch-mates.